DEVICE PHYSICS MATTERS IN RF DESIGNS AND MANUFACTURING

Chandra Gupta, Ph.D., MBA
Now with CPI, Beverly, MA
c.gupta@ieee.org

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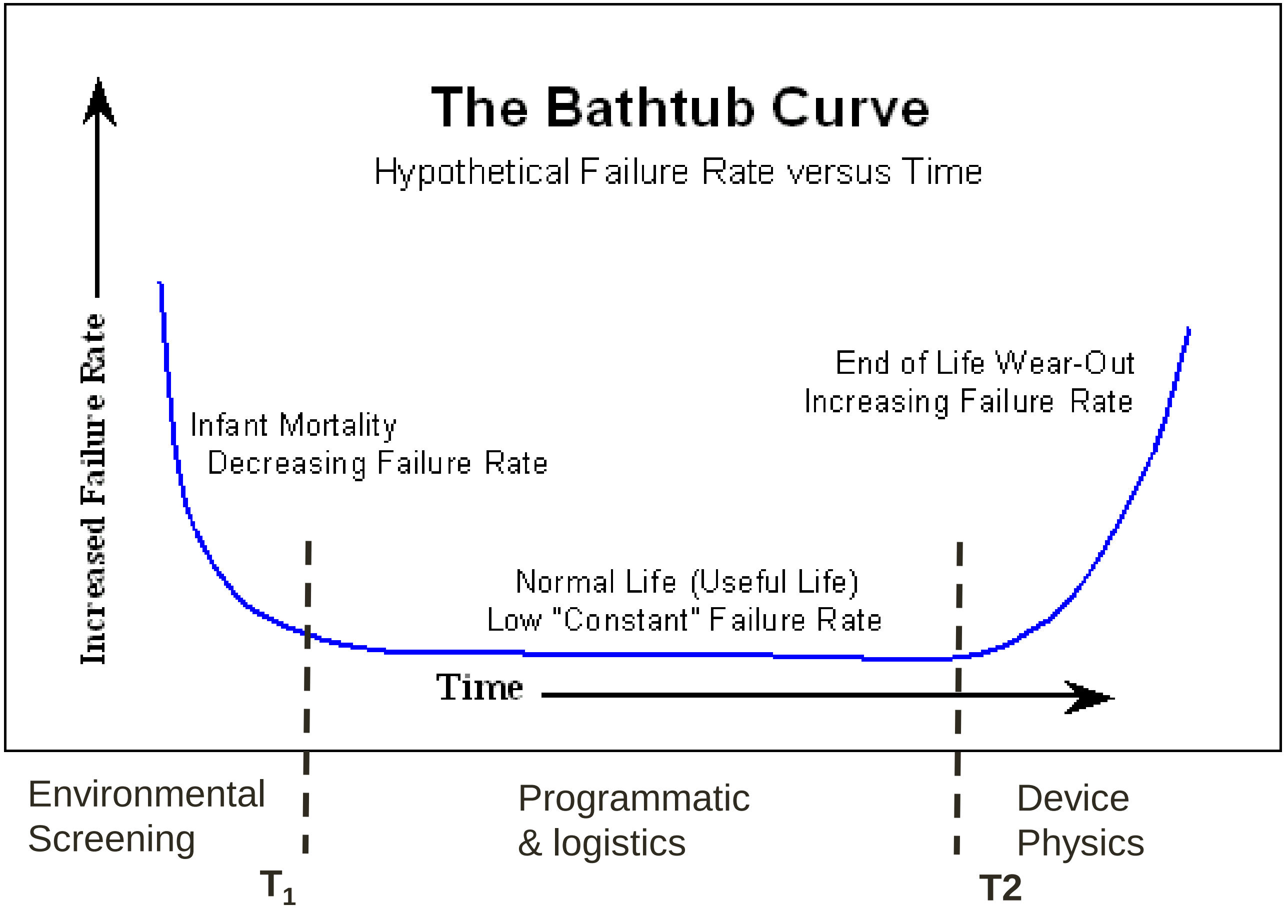
CONTENT

1.0 INTRODUCTION

INTRODUCTION

1. System in Package (SiP) have
   1. *Higher functionality*
   2. *High density of semiconductor chips Several components on a chip*
      1. *Multiple interposer boards*
      2. *Chip on chip, package on package, chip on package etc*
      3. *Several different semiconductor technologies*
   3. *Comprise of RF, analog, digital and power supply*
   4. *Multilayer and complex packaging*
2. Integration in small packages 2.5D & 3D
3. Demand longer life and full operation
4. Smaller size, lighter weight, lower power and cost effective solutions also known SWaP-C.

Failure Behavior



Reference [1]

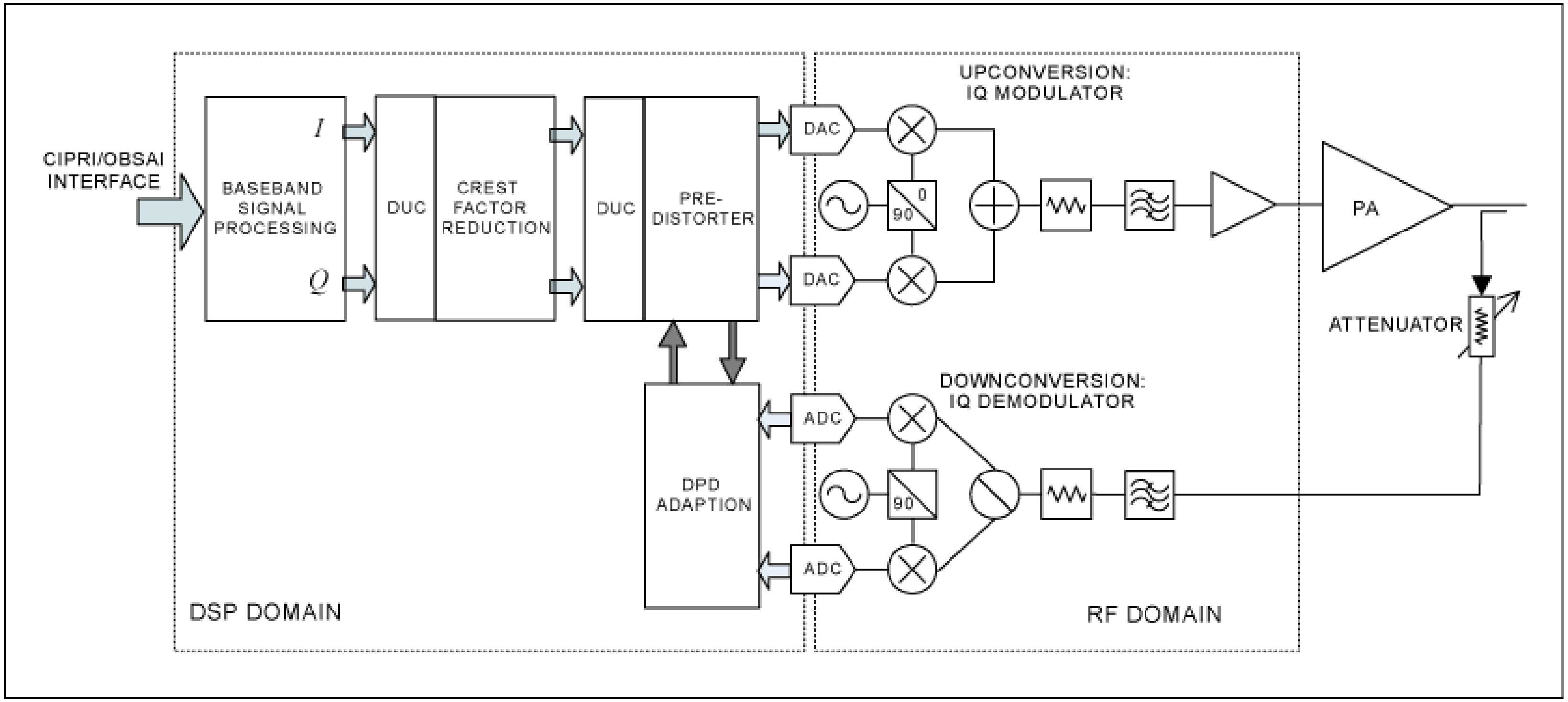
2.0 PHYSICS & DESIGN ELEMENTS

ELEMENTS

ELEMENT	DESCRIPTION
Electrical Design	Perform to the electrical performance requirements
Mechanical Design	Endure shock, vibration and other mechanical conditions
Thermal Design	Operation under all temperature conditions of use
Reliability	Mission life
Device Physics	Electro-Migration, Hot-Carrier Effects, Passivation Layer Breakdowns
Quality	Latent Failures, Process Related Defects,
Material	Kirkendall, Galvanic and Whisker Growth Effects
Processes	Ensuring construction and measurements comply with the quality and customer requirements
Parts Obsolescence	Ensuring that the part can be repaired and/or replaced over the life
Stability	Ability of the organization to service and stand behind the product
Supply Chain	Smooth and uninterrupted flow of material and services

3.0 DESIGN CHARACTERISTICS COMMONLY ADDRESSED

Example: Transmitter Module



Reference [2]

COMMONLY ADDRESSED

1. Electrical Design - simulations and prototypes
2. Package Design
3. Mechanical and Thermal Design – simulations and validations
4. Reliability Calculation – MIL Handbook, Bellcore or Telecordia
5. Process Controls – Coupon validations, SPC
6. Screening
7. Quality Compliance to Applicable Standards

4.0 INCORPORATING ADDITIONAL CONSIDERATIONS

ADDITIONAL CONSIDERATIONS

1. Commonly used design, screening and process techniques certainly are necessary and enable us to do a good job in making sure the product is satisfactory. Screening helps remove infant mortalities and reduce failure rates.
2. We need to go beyond, in order to further reduce and eliminate the end of life wear out failures during the operational life of systems with realistic physical models.

ADDITIONAL CONSIDERATIONS

These include

1. Required power on hours of operation
2. Device physics –
    1. *Activation Energy*
    2. *Electro migration*
    3. *Hot carrier injection effect*
    4. *Kirkendall Effects*
    5. *Whisker Growth*
3. ESD & EOS
4. Other effects

ARRHENIUS EQUATION

Permits one to determine reliability with thermal-stress induced failures. Established through HTOL (high Temperature Operating Life) testing.

An equation used to calculate thermal acceleration factors for semiconductor device *time-to*-failure *distributions:*

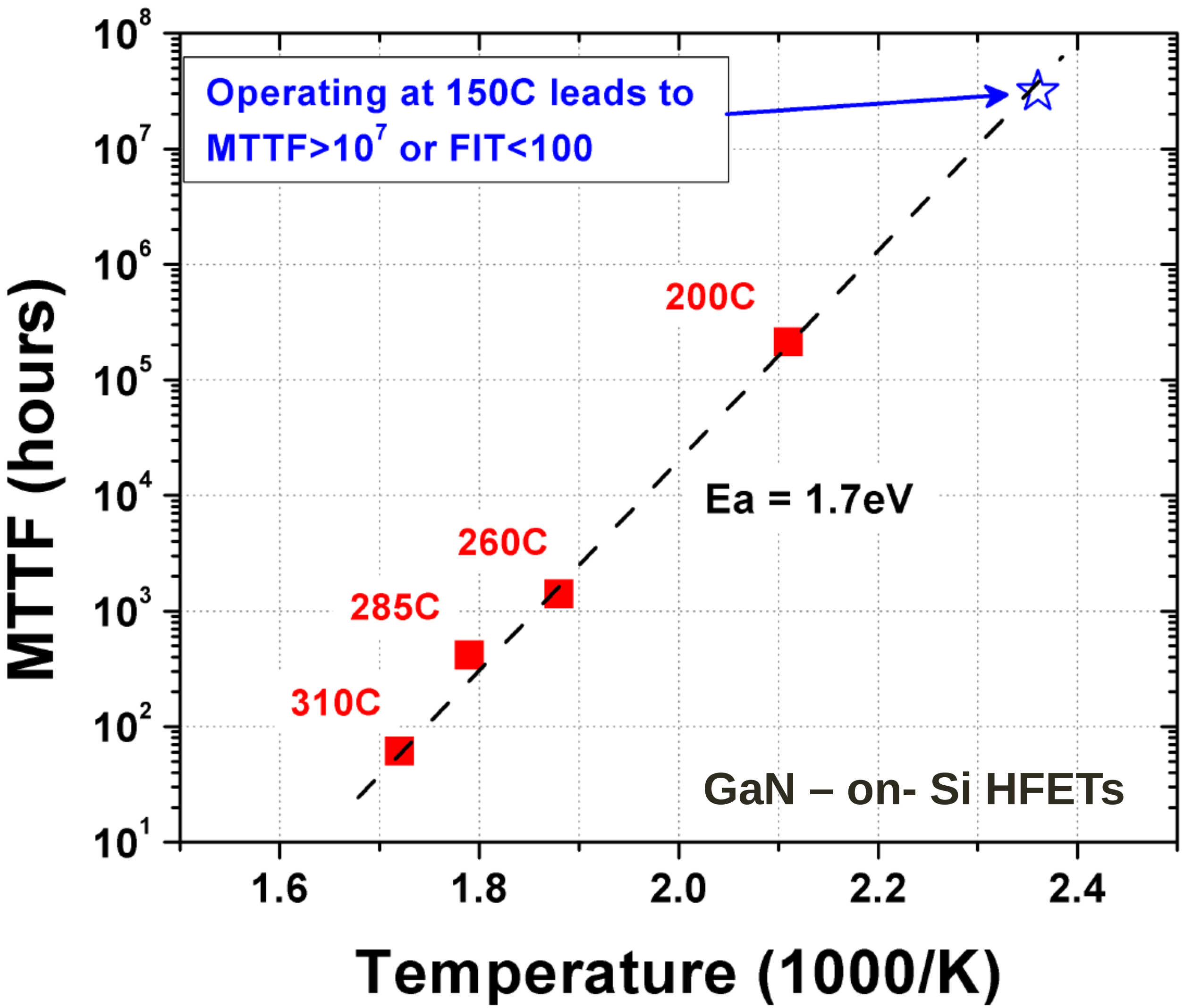
$A_T = \exp [(-E_{aa}/k) (1/T_1 - 1/T_2)]$

where

A_T is the acceleration factor due to changes in temperature;
E_{aa} is the apparent activation energy (eV);
k is Boltzmann's constant (8.62×10^{-5} eV/K);
T_1 is the absolute temperature of the test (K);
T_2 is the absolute temperature of the system (K).

Reference [3]

Example



Reference [4]

ELECTROMIGRATION

Electromigration represents degradation in metal layers with time due to electron movements under full electrical field over long term.

The effect is important in microelectronics where high direct current densities are used.

As the size in integrated circuits (ICs) decreases, the significance of this effect increases.

ELECTROMIGRATION

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$$MTTF = Aj^{-n}e^{\left(\frac{Q}{kT}\right)}$$

A is a constant
j is the current density
n is a model parameter
Q is the activation energy in eV (electron volts)
k is Boltzmann constant
T is the absolute temperature in K

1. Black's Equation models the mean time to failure (MTTF) due to electromigration.
2. Describes the failure rate dependence on the temperature, the electrical stress, and the specific technology and materials.
3. The values for *A*, *n*, and *Q* are found by fitting the model to experimental data.
4. Maps experimental data at elevated temperature and stress levels in short periods of time to expected component failure rates under actual operating conditions. HTOL testing.

Reference [5]

CARRIER INJECTION EFFECT

Hot carrier injection (HCI) is a phenomenon in solid state electronic devices where electrons or a holes gain sufficient energy to overcome a potential barrier necessary to break an interface state, resulting in loss of performance.

The term "hot" refers to the effective temperature used to model carrier density, not the overall temperature of the device.

Since the charge carriers can become trapped in the gate dielectric of a transistor, the switching characteristics of the transistor can be permanently changed.

Hot-carrier injection is one of the mechanisms that adversely affects the reliability.

Reference [6]

WHISKER GROWTH

Tin whiskers are electrically conductive, crystalline structures of tin that sometimes grow from surfaces where tin (especially electroplated tin) is used as a final finish.

Tin whiskers have been observed to grow to lengths of several millimeters (mm) and in rare instances to lengths in excess of 10 mm. Numerous electronic system failures have been attributed to short circuits caused by tin whiskers that bridge closely-spaced circuit elements maintained at different electrical potentials.

Tin is only one of several metals that is known to be capable of growing whiskers. Other examples of metals that may form whiskers include some tin alloys, Zinc, Cadmium, Indium, Antimony, Silver among others .

Reference [7]

KIRKENDALL EFFECT

Thermosonic and wedge bonding process is used to make reliable interconnections between die bond pads and leads using thin gold and copper wires.

Under thermal aging, the fine pitch gold wire ball bonds (0.6- and 0.8-mil-diameter wires) show formation of voids apart from intermetallic compound growth known as Kikendall effect.

With 1- and 2-mil-diameter gold wire bonds, the void growth is less significant and reveals fine voids.

Studies also showed that void formation is absent in the case of thicker 3-mil wire bonds.

Reference [8]

ESD & EOS EFFECTS

Electrostatic discharge (ESD) can occur in the manufacturing, shipping, receiving, and field handling of integrated circuits or computer boards with no visible signs of damage. A malfunction in these components or boards can occur immediately or the apparatus may perform for weeks, months, or even years before an unpredictable and premature breakdown causes a field failure.

Electrical Over Stress (EOS) Damage is caused by thermal overstress to a component's circuitry. The amount of damage caused by EOS depends on the magnitude and duration of electrical transient pulse widths. We can broadly classify the duration of pulse widths into long (>100 ms) and short (<100 ms) types, and magnitude into exceeding an individual component's EOS threshold.

For short pulse widths the most common failure mode is junction spiking.

For long electrical pulse widths the most common failure modes are melted metallization and open bond wires.

Reference[9]

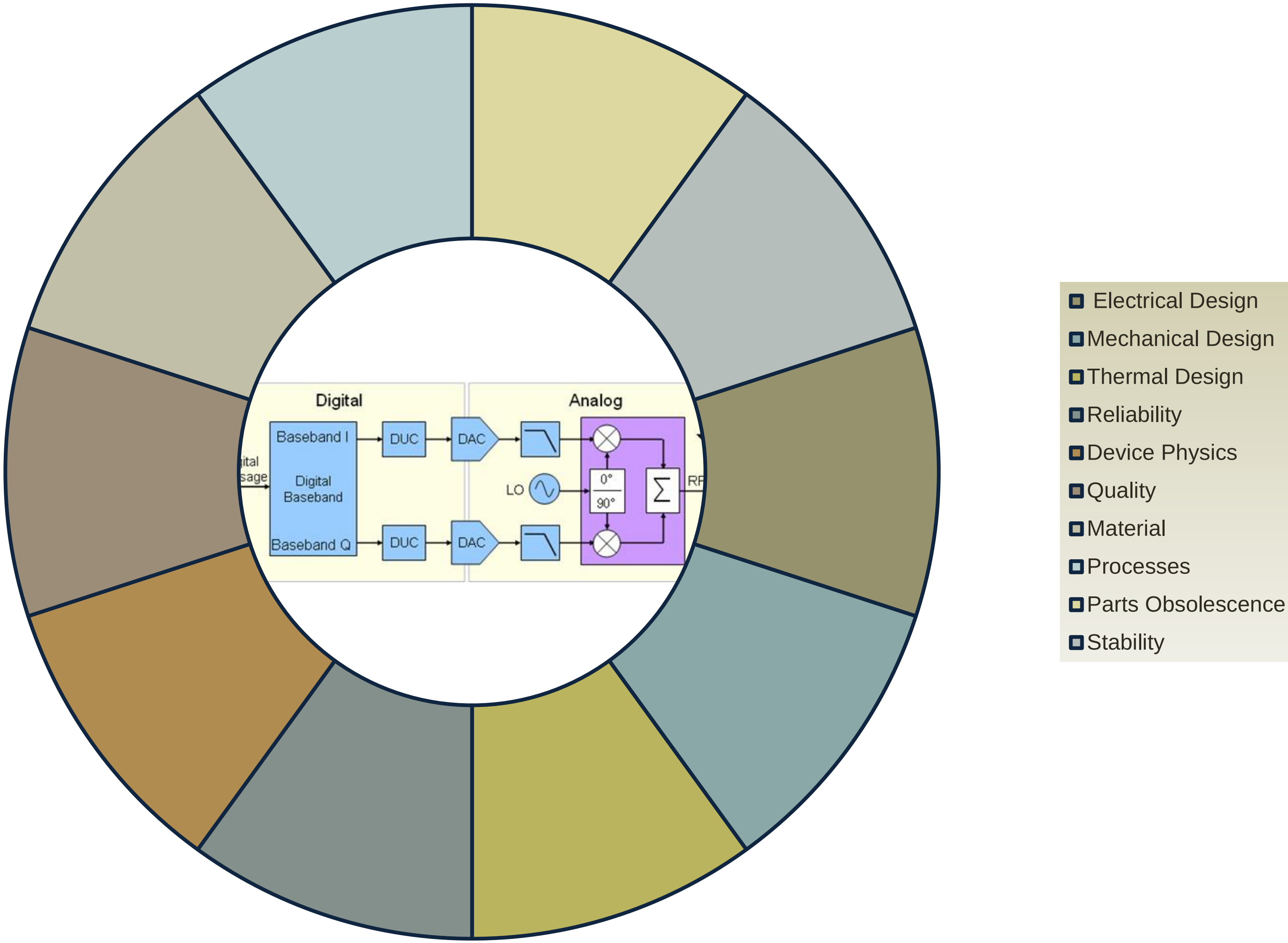
5.0 PROGRAMMATIC & LOGISTICS

Programmatic and Logistics

1. Market Dynamics
2. Parts Obsolescence
3. Supplier Stability
4. Supply Chain Management

6.0 DISCUSSION

FACTORS TO INCLUDE



DISCUSSION

- **Design considerations need to include the various physical characteristics in addition to the traditional electrical, thermal, mechanical design and processes.**
- **Device physics is vital to ensure that the wear out failures are outside the expected operational life of the system. Adequate margins need to be applied.**
- **In addition to all the design and manufacturing considerations covered here, other programmatic considerations must be managed and included in overall system deployment**
  - ***Parts Obsolescence***
  - ***Supply Chain Management***

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THANK YOU

Q&A